PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Lea et al.	Examiner: Peter L. Cheng Art Unit: 2625
Serial No.: 10/669,247	
Filed: September 24, 2003	Confirmation No.: 3532
For: **System and Method of Parallel Processing Image Data** **(as amended)**	
Date of Final Office Action: June 30, 2008	Attorney Docket No.: 200207569-1
Notice of Appeal Filed: August 19, 2008	

October 14, 2008

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is timely provided to support the Notice of Appeal filed August 19, 2008.

1. Real Party in Interest:

The real party in interest is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

2. Related Appeals and Interferences

There are no other prior and/or pending appeals, interferences, or judicial proceedings that are related to, directly affect, or that will be directly affected by or have a bearing on the Board's decision.

3. Status of Claims

Claims 1-23 are pending in the application.

Claims 1-23 stand rejected.

No claims were canceled.

No claims were allowed.

No claims were withdrawn

The rejections of claims 1-23 are appealed.

4. Status of Amendments

An After Final Amendment was filed on Sept. 10, 2008. The amendment was entered as indicated in the Advisory Action dated Oct. 2, 1008.

5. Summary of Claimed Subject Matter

Appellant notes that citations that include paragraph numbers and line numbers (e.g. [0020] lines 1-4) refer to line numbers starting at the top of the paragraph, not the top of the page.

Independent Claim 1

Claim 1 recites an image forming device (specification, page 4, paragraph [0015], lines 1-2; and figure 1, image forming device 100). The device includes a scanner (specification, page 4, paragraph [0016], lines 1-2; and figure 1, scanner 110). The scanner is configured to scan objects and generate image data representing each of the objects (specification, page 4, paragraph [0016], lines 1-3). The device also includes a memory (specification, page 5, paragraph [0018], lines 1-2; and figure 1, main memory 150). The memory is configured to store each of the image data as a page of data (specification, page 5, paragraph [0018], lines 1-3).

The device further includes a page frame memory configured to store a page of data (specification, page 6, paragraph [0022], lines 1-2; and figure 1 page frame memory 170). The page of data is copied from the memory that is to be imaged (specification, page 6, paragraph [0022], lines 3-5). An imaging mechanism is configured to receive the page of data from the page frame memory (specification, page 7, paragraph [0024], lines 1-4; and figure 1, imaging mechanism 130). The imaging mechanism generates an image from the page of data onto a print media (specification, page 4, paragraph [0015], lines 4-7; and specification, page 4, paragraph [0016], lines 9-11).

The device further includes a dual bus system (specification, page 7, paragraph [0026], lines 2-6; and figure 1, bus 155, second bus 185). The dual bus

system is configured to allow parallel transmission of data where the image data can be transmitted from the scanner to the memory simultaneously with transmitting the page of data from the page frame memory to the imaging mechanism (specification, page 7, paragraph [0026], lines 4-12).

Dependent Claim 2

Clam 2 depends from claim 1 and recites the dual bus system with a first bus connected to communicate data between the scanner and the memory (specification, page 5, paragraph [0018], lines 2-7; and figure 1, bus 155). The dual bus system also includes a second bus, independent from the first bus, connected to communicate data between the page frame memory and the imaging mechanism (specification, page 7, paragraph [0026], lines 3, 9-12; and figure 1, second bus 185).

Independent Claim 11

Claim 11 recites a method of processing image data in an image forming device (specification, page 11, paragraph [0040], lines 1-2; and figure 3, method 300). The method includes scanning sheets of print media and generating image data pages (specification, page 12, paragraph [0041], lines 2-3; and figure 3, block 305).

The method also includes loading the image data pages into a memory (specification, page 12, paragraph [0041], lines 3-4; and figure 3, block 310). The method further includes copying a first image data page into a page frame memory from the memory to prepare for imaging (specification, page 12, paragraph [0041], lines 4-5; and figure 3, method 300). The method includes transmitting the first image data page for imaging to an imaging mechanism where the transmitting

occurs in parallel with the loading (specification, page 12, paragraph [0042], lines 3-5; and figure 3, block 335).

Independent Claim 17

Claim 17 recites a system for formatting image data for an image forming device (specification, page 4, paragraph [0015], lines 1-2). The system includes a first data bus (specification, page 5, paragraph [0018], lines 3-4; and figure 1, bus 155).

The system also includes a first memory configured to store image data pages (specification, page 5, paragraph [0018], lines 2-5; and figure 1, main memory 150). The first memory is configured to receive the image data pages over the first data bus (specification, page 5, paragraph [0018], lines 2-4).

The system further includes a second memory configured to load a page of data that is to be imaged (specification, page 6, paragraph [0022], lines 1-3; and figure 1, page frame memory 170). The page of data is received from the first memory (specification, page 6, paragraph [0022], lines 4-6). A second data bus is configured to communicate the page of data from the second memory to an imaging mechanism (specification, page 7, paragraph [0026], lines 2-3, 9-11; and figure 1, second bus 185). The page of data can be transmitted to the imaging mechanism in parallel with the first memory receiving the image data pages (specification, page 7, paragraph [0026], lines 9-12).

6. Grounds of Rejection to be Reviewed on Appeal

I. Whether claims 2-4, 15 and 20 are unpatentable as being objected to because of informalities in antecedents.

II. Whether claims 1-4, 6-8, 10-12, 16-20, 22 and 23 are unpatentable under 35 U.S.C. 103(a) as being obvious over Shishizuka (US Patent No. 6,697,898 B1) (Shishizuka) in view of Westervelt (US Patent Appl. 2003/0231330 A1) (Westervelt).

III. Whether claims 5, 9, 13, 14, 15 and 21 are unpatentable under 35 U.S.C. 103(a) as being obvious over Shishizuka (US Patent 6,697,898 B1), in view of Westervelt (US Patent Appl. 2003/0231330 A1), in view of well-known prior art.

7. Argument

I. Whether claims 2-4, 15 and 20 are unpatentable as being objected to because of informalities in antecedents.

Claims 1 and 7 were amended in the Amendment After Final (9/10/2008). The amendments were entered by the examiner. In particular, claims 1 and 7 were amended to correct an antecedent: "page frame buffer" to be "page frame memory" as the examiner suggested. The amendment to claim 1 resolves the antecedents in dependent claims 2-4.

Claim 20 was amended to correct an antecedent: "a" to be "an".

Appellant believes an amendment to claim 15 was not required. Claim 15 recites: "removing an image data page from the memory after the image data page has been imaged." The antecedent to "the image data page" is in claim 15 and is correct. Accordingly, all claims comply with all requirements of 35 U.S.C. §112 and the rejection should be reversed.

The amendments were entered as indicated by the Advisory Action. However, neither the amendments nor the rejection were discussed in the Advisory Action.

II. Whether claims 1-4, 6-8, 10-12, 16-20, 22 and 23 are unpatentable under 35 U.S.C. 103(a) as being obvious over Shishizuka in view of Westervelt.

To establish a prima facie case of 35 U.S.C. §103 obviousness the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143.03. Furthermore under MPEP 2131 for a reference to anticipate a claim, "[t]he elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

As explained herein, the references fail to teach or suggest all claim elements. Furthermore, the components relied upon by the Office Action from Shishizuka and Westervelt fail to teach or suggest the claimed elements as arranged in each respective claim. Therefore, a prima facie obviousness rejection has not been established by the combined references and the rejections should be reversed.

Appellant notes that citations to the Office Action refer to the Final Office Action dated June 30, 2008.

Independent Claim 1

Claim 1 recites an image forming device comprising a scanner, a memory, a page frame memory, an imaging mechanism, and a dual bus system with a specific configuration. Shishizuka fails to teach or suggest the claimed image forming device and dual bus system as alleged by the Office Action.

Claim 1 recites the dual bus system as:

> "a dual bus system configured to allow parallel transmission of data where the image data can be transmitted from the scanner to the memory simultaneously with transmitting the page of data from the page frame memory to the imaging mechanism."

As recited, there are two data transmission paths formed by the dual bus system: one bus is connected so that image data is transmitted (1) from the scanner to the memory, and another bus allows simultaneously transmission of the page of data (2) from the page frame memory to the imaging mechanism. This arrangement of elements, connections therebetween, and configuration of the dual bus is not taught or suggested by the references.

The Office Action cites the "DoEngine" of Shishizuka as teaching the claimed dual bus system. Within the DoEngine (which is best seen in Figure 4), the Office Action cites two buses, the G bus 404 and the B bus 405. (Office Action, page 5). However, the DoEngine fails to teach the claimed configuration. The G bus 404 transmits data between the scanner controller 4302 to the cache memory 403 (via system bus bridge 402), and the B bus transmits data from the cache memory 403 to the printer controller 4303 (via system bus bridge 402). A page frame memory (being a separate element from the cache memory 403) is not present and not part of the G bus and B bus configuration. Thus, the claimed page frame memory and the claimed arrangement with the recited dual bus system are not taught or suggested by the G and B buses of Shishizuka. Shishizuka fails to support a prima facie obviousness rejection. The rejection is improper and should be reversed.

The Office Action then cites different components from Shishizuka as being a first and second bus that teach the claimed dual bus system (OA, page 7 last paragraph). In particular, the Office Action states:

> Therefore, SHISHIZUKA teaches a first bus (i.e., from the interface "VIDEO I/F TO SCANNER" to the "Scanner Controller" 4302 to either of the G bus or B bus (by means of a "G Bus/B Bus I/F" 4301A) which is connected to SDRAM by means of a "System Bus Bridge" 402, "MC Bus", "SDRAM & ROM Controller (MC)" 403, and "Memory BUS", all shown in Fig. 4) which connects the "scanner to the memory" and a second bus (i.e., from the "Printer Controller" 4303 containing the printer controller FIFO to the printer and is shown as "VIDEO I/F TO PRINTER" in Fig. 4) which connects the "page frame buffer to the imaging mechanism". Data can be transmitted from the scanner to memory while simultaneously transmitting data from the page frame buffer to the printer.]
>
> (OA, page 7-8) [emphasis in original]

Appellant notes that the "I/F" elements referred to by Shishizuka are interface ports, not a bus (Shishizuka, col. 35, lines 54-56: "The scanner device I/F is an input/output port..."). Figure 45 of Shishizuka discloses the scanner video I/F connections and components. Figures 66-67 disclose the printer controller 4303 components and connections including the printer device I/F. The multiple components involved and multiple communication channels therebetween (e.g. different signal paths) are shown to pass different signals between each other over the different communication channels. This is a hodgepodge of components that fails to teach or suggest to one of ordinary skill in the art the actual claimed configuration. The claim is thus not taught or suggested and the rejection should be reversed.

Additionally, the conclusion made by the examiner in the last sentence from the cited text above, that "[d]ata can be transmitted from the scanner to memory while simultaneously transmitting data from the page frame buffer to the printer" is not supported by Shishizuka and no citation to an actual teaching or suggestion in Shishizuka is provided (OA, page 8, lines 1-2). Accordingly, Shishizuka fails to teach or suggest the elements relied upon by the rejection and fails to teach or suggest the claim. Shishizuka fails to support a prima facie obviousness rejection and the rejection should be reversed.

The "Response to Arguments" section on page 29 of the Final Office Action adds new citations to columns 73 and 74 of Shishizuka as teaching the claimed buses and parallel transmission of data. However, the actual claimed elements are still not taught or suggested. For example, col. 73, lines 31-33 state that the bus "allows accessing the CPU and memory in parallel", but claim 1 does not recite accessing a CPU and memory in parallel. Claim 1 defines a configuration with a first bus between a scanner and memory, and a second bus between a page frame memory and an imaging mechanism. Thus claim 1 is not taught or suggested. Furthermore, the examiner cites col. 73, lines 33-34 that state: "Data can be output in parallel with input of data." This means that the scanner itself is scanning at the same time that the printer is printing. However, the claim recites a configuration internal and in-between the scanner and printer, not the operation of the scanner and printer. Thus the cited section fails to teach or suggest the claim.

The Final Office Action on page 29 also cites Shishizuka col. 73, lines 44-46. This section refers to Fig. 113B and describes the "assignment and release of a device" (col. 73, lines 41-42). It describes the operation of the scanner and printer as devices. Thus this section describes the operation of the scanner scanning and the printer printing in parallel. And as stated in the previous paragraph, claim 1 recites a configuration internal and in-between the scanner and printer, not the operation of the scanner and printer themselves. Thus the cited sections fail to teach or suggest the claim. Shishizuka fails to support a prima facie obviousness rejection.

Shishizuka's VSYNC and HSYNC Timing Signals

The Office action relies upon Shishizuka's discussion of vertical synchronous signals (VSYNC) to the printer, horizontal synchronous signals (HSYNC), and a video clock (Office Action, pages 6-7). Appellant respectfully submits the VSYNC and HSYNC signals are not relevant to the claim language.

These are timing signals to synchronize the scanner device and printer device vertically and horizontally (col. 65, lines 10-30). How the VSYNC and HSYNC signals are processed fail to teach or suggest simultaneous or parallel transmission of data by a dual bus transferring data from page frame memory to the imaging mechanism while also transferring image data from a scanner to main memory. Thus, this cited section of Shishizuka (col. 66, lines 58-67) is not on point and fails to support the rejection.

Additionally, the paragraph following col. 66, lines 58-67 describes the data flow of the image data and describes it as "the image data flows in a sequence..." (col. 67, lines 1-12). Parallel transmission of data as claimed is not taught or suggested. Therefore again, Shishizuka fails to teach or suggest the claim and the rejection should be reversed.

Westervelt Reference

The Office Action identifies a deficiency in Shishizuka as not teaching a page frame buffer configured to store a page of data and cites Westervelt's first-in-first-out FIFO buffer 353 to cure the deficiency (Office Action, page 8). The combination still fails to teach or suggest the claimed elements. Simply adding a FIFO buffer to Shishizuka does not cure the fact that the claimed dual bus and the claimed arrangement of components are not taught or suggested by either reference, alone or in combination.

Furthermore, Westervelt fails to teach or suggest to one of ordinary skill how its FIFO buffer would be connected and where it would be connected into the DoEngine of Shishizuka. Indeed, the DoEngine already includes a cache memory 403 (figure 4) and the printer controller 4303 already includes a FIFO buffer 6608 (figure 66). One of ordinary skill in the art would have no reason to add another buffer to the DoEngine of Shishizuka. Adding a buffer would increase cost, would

further complicate the circuit, and would require reconfiguration of the components and signal paths. Thus the motivation to combine provided by the Office Action (page 8, 3rd parag.) is not supported by the references and contradicts the actual result of the proposed modification. Instead the combination is made only by impermissible hindsight using the claims as a blueprint. The rejection is improper.

Accordingly, a prima facie obviousness rejection has not been established. The rejection is improper and should be reversed. As such, the rejection of dependent claims 2-10 are also improper and should be reversed. Claim 1 patently distinguishes over the references of record and should now be allowed.

Dependent Claim 2

Claim 2 recites that the dual bus system includes a first bus connected to communicate data between the scanner and the memory, and a second bus, independent from the first bus, connected to communicate data between the page frame memory and the imaging mechanism. The office action relies on Shishizuka based on the alleged first and second buses as asserted under claim 1 (Office Action, bottom of page 8-9. As explained above, no such first or second bus is taught or suggested in the manner claimed or connected between the recited elements. A prima facie obviousness rejection has not been established. Thus the rejection of claim 2 is improper and should be reversed.

Independent Claim 11

The Office Action on page 13 states that the recited claim language of "transmitting the first image data page for imaging to an imaging mechanism where the transmitting occurs in parallel with the loading" is taught by Shishizuka in the following section:

> Simultaneously, the printer controller (PRC) outputs the vertical synchronous signal (VSYNC) to the printer. Thereafter, the horizontal synchronous signal (HSYNC) and the video clock are input from the printer. In synchronization with the HSYNC and the video clock, the printer controller outputs the image data from the internal FIFO to the printer. (Shishizuka , col. 66, lines 62-67)

The HSYNC and VSYNC timing signals were discussed under claim 1. These timing signals are irrelevant to the claim language. Appellant respectfully submits that the cited text teaches outputting image data from the printer controller in synchronization with the HSYNC and VSYNC timing signals. The timing signals are not image data pages that are generated from scanning sheets of print media as recited in the claim. Also, the timing signals are not image data pages loaded into a memory.

As such, the VSYNC and HSYNC timing signals, as well as the processing of the timing signals, are irrelevant to the claimed elements. Thus, the cited text fails to teach or suggest "transmitting the first image data page for imaging to an imaging mechanism where the transmitting occurs in parallel with the loading" as recited in claim 11. Accordingly, Shishizuka fails to teach or suggest the elements relied upon by the rejection and fails to support a prima facie rejection. The rejection should be reversed.

Furthermore, the Office Action relies on Westervelt for teaching the element of copying a page into a page frame memory. In view of the deficiencies of Shishizuka and the deficiencies in combining Westervelt and Shishizuka as explained under claim 1, Westervelt fails to cure the deficiencies of Shishizuka.

Therefore the combined references still fail to establish a prima facie obviousness rejection. The rejection is improper and should be reversed. Claim 11 should now be allowed. Accordingly, the rejection of dependent claims 12-16

are also improper and should be reversed. All claims are now in condition for allowance.

Independent Claim 17

Claim 17 was rejected based on similar reasoning as applied against claim 1 (Office Action, starting on page 16). As explained under claim 1, the examiner's reliance on Shishizuka is not on point and does not teach the bus structure as claimed. Thus, Shishizuka fails to teach or suggest the recited arrangement of a first data bus, a second data bus, a first memory, a second memory, and parallel transmission of data between components as recited in claim 17.

Furthermore, the Office Action's reliance on Westervelt for teaching a FIFO buffer is not sufficient to cure the deficiencies of Shishizuka. As explained under claim 1, the combined references still fail to establish a prima facie obviousness rejection. The rejection is improper and should be reversed. Claim 17 should now be allowed. Accordingly, the rejection of dependent claims 18-23 are also improper and should be reversed. All claims are now in condition for allowance.

III. Whether claims 5, 9, 13, 14, 15 and 21 are unpatentable under 35 U.S.C. 103(a) as being obvious over Shishizuka in view of Westervelt, in view of well-known prior art.

Claims 5, 9, 13, 14, 15 and 21 are dependent claims. Since the rejection of their respective independent claims has been shown to be unsupported and improper, then the rejection of the dependent claims is also improper. Shishizuka and Westervelt combined fail to establish a prima facie obviousness rejection of any claim.

For each claim, the examiner has relied on what is "well-known" prior art but has not provided any basis to support such a conclusion. Thus, Official Notice has in effect been taken. The examiner's conclusion is not capable of "instant and unquestionable demonstration as being well-known" as required by MPEP 2144.03. Thus the rejections are improper and should be reversed.

MPEP 2144.03 states:

> Official notice without documentary evidence to support an examiner's conclusion is permissible only in some circumstances. While "official notice" may be relied on, these circumstances should be rare when an application is under final rejection or action under 37 CFR 1.113. Official notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known. (MPEP 2144.03, section A, 1st parag.)
>
> It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known. (MPEP 2144.03, section A, 2nd parag.)
>
> It is never appropriate to rely solely on "common knowledge" in the art without evidentiary support in the record, as the principal evidence upon which a rejection was based. *Zurko*, 258 F.3d at 1385, 59 USPQ2d at 1697 ("[T]he Board cannot simply reach conclusions based on its own understanding or experience-or on its assessment of what would be basic knowledge or common sense. Rather, the Board must point to some concrete evidence in the record in support of these findings.").
> (MPEP 2144.03, section A, 3rd parag.)

Appellant disputes that the claimed elements are well known. Authority must be produced to support the rejection. The rejection fails to point to concrete evidence in the record to support its findings. Thus the rejection fails to meet with the stringent standards as required by MPEP 2144. The rejection is improper and should be reversed.

Conclusion

For the reasons set forth above, a prima facie obviousness rejection has not been established for any claim. All rejections have been shown to be improper. Appellant respectfully believes that all pending claims 1-23 patentably and unobviously distinguish over the references of record and that the rejections should be withdrawn. Appellant respectfully requests that the Board of Appeals overturn the Examiner's rejections and allow all pending claims. An early allowance of all claims is earnestly solicited.

Respectfully submitted,

OCT. 14, 2008

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8. Claims Appendix

1. An image forming device comprising:

a scanner configured to scan one or more objects and generate image data representing each of the one or more objects;

a memory configured to store each of the image data as a page of data;

a page frame memory configured to store a page of data, copied from the memory, that is to be imaged;

an imaging mechanism configured to receive the page of data from the page frame memory and generate an image from the page of data onto a print media; and

a dual bus system configured to allow parallel transmission of data where the image data can be transmitted from the scanner to the memory simultaneously with transmitting the page of data from the page frame memory to the imaging mechanism.

2. The device of claim 1 where the dual bus system includes a first bus connected to communicate data between the scanner and the memory, and a second bus, independent from the first bus, connected to communicate data between the page frame memory and the imaging mechanism.

3. The device of claim 2 where the first bus is configured to allow image data to be loaded into the memory independent of transmitting data from the page frame memory to the imaging mechanism.

4. The device of claim 2 further comprising:

a first processor configured to control communication of the image data to the memory; and

a second processor configured to control communication of the page of data from the page frame memory to the imaging mechanism.

5. The device of claim 4 where the second processor is configured to decompress the page of data and transmit pulse modulated wave patterns to the imaging mechanism based on the decompressed page of data.

6. The device of claim 4 where the first and second processors include application specific integrated circuits.

7. The device of claim 1 where the page frame memory is configured to store one or more pages of data as one or more units.

8. The device of claim 1 where the dual bus system is configured to communicate data by direct memory access.

9. The device of claim 1 further including a storage device configured to store image data from the scanner once the memory is full.

10. The device of claim 1 where the page of data includes at least three planes of color data.

11. A method of processing image data in an image forming device, the method comprising:

scanning one or more sheets of print media and generating one or more image data pages;

loading the one or more image data pages into a memory;

copying a first image data page into a page frame memory from the memory to prepare for imaging; and

transmitting the first image data page for imaging to an imaging mechanism where the transmitting occurs in parallel with the loading.

12. The method of claim 11 further including converting the first image data page into print ready data before transmitting for imaging.

13. The method of claim 11 further including holding the first image data page in the page frame memory until the imaging mechanism is ready to print.

14. The method of claim 11 further including loading one or more image data pages into a mass storage device once the memory is full.

15. The method of claim 11 further including removing an image data page from the memory after the image data page has been imaged and outputted from the image forming device.

16. The method of claim 11 further including sequentially copying the one or more image data pages from the memory to the page frame memory to prepare for imaging.

17. A system for formatting image data for an image forming device, the system comprising:

a first data bus;

a first memory configured to store image data pages, the first memory being configured to receive the image data pages over the first data bus;

a second memory configured to load a page of data that is to be imaged, the page of data being received from the first memory; and

a second data bus configured to communicate the page of data from the second memory to an imaging mechanism where the page of data can be transmitted to the imaging mechanism in parallel with the first memory receiving the image data pages.

18. The system as set forth in claim 17 further including an imaging processor configured to process the page of data from the second memory into print ready data that can be processed by the imaging mechanism.

19. The system as set forth in claim 18 where the imaging processor includes one or more logic circuits each configured to process one plane of color data from the page of data.

20. The system as set forth in claim 17 where the first data bus is in data communication with a scanning device configured to scan objects and generate an image data page including color data representing each scanned object.

21. The system as set forth in claim 17 further including a storage disk device configured to store overflow image data pages after the first memory is at capacity.

22. The system as set forth in claim 17 where the system is configured to copy an image data page from the first memory to the second memory by direct memory access.

23. The system as set forth in claim 17 where the system is configured to process image data pages as one or more data units.

9. Evidence Appendix

None. There is no extrinsic evidence.

10. Related Proceedings Appendix

None. There are no related proceedings.